In the Claims:

1-19 (Canceled)

20. (Currently Amended) A method of fabricating a transistor, the method comprising:

providing a workpiece;

depositing a gate dielectric material over the workpiece;

depositing a gate material over the gate dielectric material;

patterning the gate material and the gate dielectric material to form a gate and a gate dielectric over a channel region of the workpiece;

forming a first recess in a source region of the workpiece and a second recess in a drain region of the workpiece, the source region and the drain region being ~~proximate and~~ separated by the channel region;

filling the first recess and the second recess with a dopant-bearing metal; and

annealing the workpiece to cause diffusion of a dopant of the dopant-bearing metal into the workpiece and form a doped region within the workpiece adjacent the dopant-bearing metal in the source region and the drain region.

21. (Original) The method according to Claim 20, wherein annealing the workpiece comprises a temperature of about 900 °C or less for about 1 hour or less.

22. (Original) The method according to Claim 20, wherein the gate dielectric comprises sidewalls, wherein filling the first recess and the second recess with the dopant-bearing metal comprises:

depositing the dopant-bearing metal over the first recess, the second recess, the gate, and the sidewalls of the gate dielectric; and

removing the dopant-bearing metal from over the gate and sidewalls of the gate dielectric, leaving the dopant-bearing metal in the first recess and the second recess.

23. (Original) The method according to Claim 20, wherein the gate and the gate dielectric comprise sidewalls, further comprising forming a first spacer on the sidewalls of the gate and the gate dielectric, before forming the first recess and the second recess.

24. (Original) The method according to Claim 23, wherein forming the first spacer comprises forming a spacer comprising a width of about 20 Å to about 70 Å.

25. (Original) The method according to Claim 23, further comprising implanting ions of a dopant into the source region and the drain region, after forming at least the first spacer, and annealing the workpiece to form deep implantation regions in the source region and the drain regions beneath the doped regions.

26. (Original) The method according to Claim 23, wherein the first spacer comprises sidewalls, further comprising forming a second spacer over the sidewalls of the first spacer, after annealing the workpiece.

27. (Original) The method according to Claim 26, further comprising implanting ions of a dopant into the source region and the drain region, after forming the second spacer, and annealing the workpiece to form deep implantation regions in the source region and the drain regions beneath the doped regions.

28. (Original) The method according to Claim 20, wherein forming the first recess and the second recess comprise forming recesses having a depth of about 200 Å or less.

29. (Original) The method according to Claim 28, wherein filling the first recess and the second recess with a dopant-bearing metal comprises filling the first recess and the second recess with TiB_2, ZrB_2, HfB_2, ZrP, TiP, $ZrSb_2$, $TiSb_2$, $HfSb_2$, or arsinides of Zr or Hf.

30. (Original) The method according to Claim 20, wherein forming the first recess and the second recess comprise a single patterning step.

31. (Original) The method according to Claim 20, wherein depositing the gate dielectric material comprises depositing HfO_2, $HfSiO_X$, Al_2O_3, ZrO_2, $ZrSiO_X$, Ta_2O_5, La_2O_3, SiO_2, Si_xN_y, SiON, or combinations thereof.

32. (New) A method of forming a transistor, the method comprising:

providing a semiconductor body;

forming a gate dielectric over a channel region that is located in the semiconductor body;

a gate disposed over the gate dielectric; and

forming a source and a drain in a semiconductor body so that the source and drain are separated by the channel region, wherein the source and drain each comprise a dopant-bearing metal region disposed within a top surface of the semiconductor body and a doped region disposed in the semiconductor body adjacent the dopant-bearing metal region.

33. (New) The method of claim 32, wherein the dopant-bearing metal regions comprise a thickness of about 200 Å or less.

34. (New) The method of claim 32, wherein the dopant-bearing metal regions comprise a at least one material selected from the group consisting of TiB_2, ZrB_2, HfB_2, ZrP, TiP, $ZrSb_2$, $TiSb_2$, $HfSb_2$, an arsenide of Zr, and an arsenide of Hf.

35. (New) The method of claim 32, wherein forming a source and a drain comprise forming a region that includes boron.

36. (New) The method of claim 32, wherein forming a source and a drain comprise forming a region that includes phosphorus.

37. (New) The method of claim 32, wherein forming a source and a drain comprise forming a region that includes arsenic.

38. (New) The method of claim 32, wherein forming a source and a drain comprise forming a region that includes antimony.

39. (New) The method of claim 32, wherein forming a gate dielectric comprises forming a layer of a high dielectric constant material.

40. (New) The method of claim 39, wherein the high dielectric constant material comprises HfO_2, $HfSiO_X$, Al_2O_3, ZrO_2, $ZrSiO_X$, Ta_2O_5, La_2O_3 or combinations thereof.

41. (New) The method of claim 32, wherein forming the source and the drain comprises performing a deep implantation.

42. (New) A method of fabricating a transistor, the method comprising:

providing a semiconductor body;

depositing a gate dielectric material over the semiconductor body;

depositing a gate material over the gate dielectric material;

patterning the gate material and the gate dielectric material to form a gate and a gate dielectric over a channel region of the semiconductor body;

depositing a dopant-bearing metal over the semiconductor body in regions adjacent the gate; and

annealing the workpiece to cause diffusion of a dopant of the dopant-bearing metal into the semiconductor body.

43. (New) The method of claim 42 wherein depositing a gate dielectric material comprises depositing a high dielectric constant material.

44. (New) The method of claim 43 wherein depositing a gate material comprises depositing a metal.

45. (New) The method of claim 42 wherein the dopant-bearing comprises at least one material selected from the group consisting of TiB_2, ZrB_2, and HfB_2

45. (New) The method of claim 42 wherein the dopant-bearing comprises at least one material selected from the group consisting of ZrP and TiP.

46. (New) The method of claim 42 wherein the dopant-bearing comprises at least one material selected from the group consisting of $ZrSb_2$, $TiSb_2$, and $HfSb_2$.

47. (New) The method of claim 42 wherein the dopant-bearing comprises an arsenide of Zr or an arsenide of Hf.